Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 12 of 12 returned.

☐ 1. Document ID: US 20040002930 A1

Using default format because multiple data bases are involved.

L9: Entry 1 of 12 File: PGPB Jan 1, 2004

PGPUB-DOCUMENT-NUMBER: 20040002930
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040002930 A1

TITLE: Maximizing mutual information between observations and hidden states to minimize classification errors

PUBLICATION-DATE: January 1, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Oliver, Nuria M.	Kirkland	WA	US	
Garg, Ashutosh	Urbana	IL	US	

US-CL-CURRENT: 706/46; 706/20, 706/21

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20030164835 A1

L9: Entry 2 of 12 File: PGPB Sep 4, 2003

DOCUMENT-IDENTIFIER: US 20030164835 A1
TITLE: System and method for performing predictable signature analysis

Abstract Paragraph:
In one embodiment, a computer system includes a first component configured to output data on a bus in response to a request for data from a second component. The data output by the first component may include both the requested data and unrequested data, and the unrequested data may have an unpredictable value. A controller coupled to the bus may be configured to replace the unrequested data with data that has a predictable value. A signature analysis register included in the second component is configured to capture the requested data and the predictable data output by the controller. Thus, the signature captured in the second component may be predictable, despite the unpredictable data output by the first component.

h e b b g e e e f e e ef b e

Summary of Invention Paragraph:
[0007] Various embodiments of a system and method for performing predictable signature analysis are disclosed. In one embodiment, a computer system includes a first component configured to output data on a bus in response to a request for data from a second component. The data output by the first component may include both the requested data and unrequested data, and the unrequested data may have an unpredictable value. A controller coupled to the bus may be configured to replace the unrequested data with data that has a predictable value. A signature analysis register included in the second component is configured to capture the requested data and the predictable data output by the controller. Thus, the signature captured in the second component may be predictable, despite the unpredictable data output by the first component.

Detail Description Paragraph:
[0094] FIG. 9 shows one embodiment of a method of performing signature analysis. In this embodiment, a requesting device requests data at 901. A providing device provides data to the requesting device in response to the request, as indicated at 903. If the providing device is providing unrequested data to the requesting device (e.g., invalid data bytes identified by a byte mask corresponding to the data being provided), the unrequested data may be replaced with data having a known value (e.g., zero), as indicated at 905 and 907. The modified data may then be provided to the requesting device and captured by an SAR associated with the requesting device. Thus, the unrequested data, which may have an upredictable value that causes the signature captured in 909 to be unpredictable, is replaced with a predictable value that causes the signature captured at 909 to be predictable.

CLAIMS:

1. A computer system comprising: a host computer system; a first component configured to output data, wherein the data includes requested data and unrequested data; a second component configured to request data from the first component, wherein the second component includes a signature analysis register configured to capture data, wherein the signature analysis register is configured to be controlled by the host computer system; a bus coupling the first component and the second component and configured to transmit data between the first component and the second component; and a controller coupled to receive the data and the unrequested data output by the first component, wherein the controller configured to receive the data output by the first component in response to the second component's request, wherein the controller is configured to replace the unrequested data with predictable data and to output the predictable data and the requested data, wherein the signature analysis register is configured to capture the predictable data and the requested data.

10. A graphics system comprising: a first component configured to output data, wherein the data includes requested data and unrequested data; a second component configured to request data from the first component, wherein the second component includes a signature analysis register configured to capture data; a bus coupling the first component and the second component and configured to transmit data between the first component and the second component; and a controller coupled to receive the requested data and the unrequested data output by the first component, wherein the controller configured to receive the data output by the first component in response to the second component's request, wherein the controller is configured to replace the unrequested data with predictable data and to output the predictable data and the requested data, wherein the signature analysis register is configured to capture the predictable data and the requested data.

21. A method of performing signature analysis, the method comprising: a requesting device requesting data; a providing device providing data in response to said requesting, wherein the data comprises requested data and unrequested data;

replacing the unrequested data with predictable data, wherein the predictable data has a predictable value; and a signature analysis register in the requesting device capturing the predictable data and the requested data.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

3. Document ID: US 20030053358 A1

L9: Entry 3 of 12 File: PGPB Mar 20, 2003

DOCUMENT-IDENTIFIER: US 20030053358 A1
TITLE: Dft technique for avoiding contention/conflict in logic built-in self-test

Abstract Paragraph:
A packaged component includes a pattern generator for generating successive random data patterns. The component further includes a programmable constraint correction module, coupled to the pattern generator, to replace undesirable random data patterns with desirable bit sequences to overcome bus contention problems in the generated random data patterns. The component further includes an integrated circuit device to be functionally tested. The device receives the constrained random data patterns from the constraint correction module and outputs a test result. The device further includes a programmable X-masking module coupled to the device receives and masks the test result by replacing unpredictable bit values in the received test result with predictable bit values. A signature analyzer coupled to the X-masking module receives the masked test result and compresses the test result into a signature. Then a comparator coupled to the signature analyzer compares the signature with a predetermined test result to determine whether the device is free of structural defects.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

4. Document ID: US 6510398 B1

L9: Entry 4 of 12 File: USPT Jan 21, 2003

DOCUMENT-IDENTIFIER: US 6510398 B1
TITLE: Constrained signature-based test

Abstract Text (1):
A test system for structurally testing an integrated circuit device includes a pattern generator for generating successive random data patterns (scan chain). The test system further includes a constraint checker and corrector module, coupled to the pattern generator, to replace undesirable random data patterns (state elements joined together in the scan chain such that one state element is connected to a ground and the other state element is connected to a power supply) with desirable bit sequences to eliminate bus contention problems in the generated random data patterns. The test system further includes the integrated circuit device to be

tested. The integrated circuit device receives the constrained random data patterns from the constraint checker and corrector module and outputs a test result. The test system further includes an X-masking module coupled to the integrated circuit device. The X-masking module receives the test result from the integrated circuit device, and it masks the test result by replacing unpredictable bit values (these are bit values generated due to not scanning some state elements in the scan chain) in the test result with predictable bit values. A signature analyzer coupled to the X-masking module receives the masked test result and compress the test result into a signature. Then a comparator coupled to the signature analyzer compares the signature with a predetermined test result to determine the functionality of the integrated circuit device.

CLAIMS:

13. A method of testing an integrated circuit device comprising: generating constrained random data patterns by constraining undesirable random data patterns in generated random data patterns with desirable bit sequences; inputting the constrained random data patterns into the integrated circuit device; testing the integrated circuit device using the constrained random data patterns; receiving a test result; inputting the received test result into a signature analyzer; compressing the test result by masking unpredictable bit values with predictable bit values in the test result and outputting a signature of the test result; comparing the signature to a predetermined test result; and determining whether the integrated circuit device is functioning properly based on an outcome of the comparison.

19. A system for structurally testing an integrated circuit device comprising: an external pattern generator to generate successive random data patterns; an external constraint checker and corrector module, coupled to the pattern generator, to constrain nodes/elements in the random data pattern generated by the pattern generator; an integrated circuit device including circuitry, coupled to the constraint checker and corrector module, to receive the constrained random data pattern and to output a test result; an X-masking module, coupled to the integrated circuit device, to mask the outputted test result from the integrated circuit device by replacing any unpredictable bit values with predictable bit values in the test result; and a signature analyzer, coupled to the X-masking module, to compress the masked test result into a signature.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

---

☐ 5. Document ID: US 6051987 A

L9: Entry 5 of 12 File: USPT Apr 18, 2000

DOCUMENT-IDENTIFIER: US 6051987 A
TITLE: Apparatus and method for detection of residual magnetic fields in dynamoelectric machines

Brief Summary Text (5):
Various technologies are known in the art to minimize the negative impact motor failures have on the safety, reliability, and production of motors. While some of these known methods have employed undesirable destructive testing techniques, others use non-destructive techniques to test stators and rotors for defects. One

such test measures inductance versus rotor position. According to this test, the rotor is slowly turned while a known electrical signal is applied to the inductive windings of a motor. The known signal is reflected as an electromagnetic field. The manner in which characteristics, such as frequency, amplitude and waveform, of an applied field are reflected represents an electromagnetic signature of a particular motor. This electromagnetic signature is analyzed to detect dissymmetries, which can be used to predict defects in the motor. The electromagnetic signature can also be chronicled against historical motor data to predict future motor failures.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. D

6. Document ID: US 6041426 A

L9: Entry 6 of 12 File: USPT Mar 21, 2000

DOCUMENT-IDENTIFIER: US 6041426 A

**** See image for Certificate of Correction ****

TITLE: Built in self test BIST for RAMS using a Johnson counter as a source of data

Brief Summary Text (6):

Conventional BIST designs typically utilize relatively complex techniques for generating data and predicting failure, usually involving collection of a signature for analysis. Furthermore, most BIST designs do not provide for detection of multibit faults. Above-cited related application Ser. No. 08/502,574 discloses a BIST system in which multiple embedded RAMs are sequentially tested for stuck at faults, including multibit faults. Parity for the RAMs is also tested and marginal read/write problems are tested by changing clock frequency. A lockup mechanism yields the identity of the failed bits. A counter is utilized to iteratively cycle through the full address range of a RAM under test, performing write/read/compare operations. After one RAM has been tested, the counter increments to select another RAM for testing. This procedure is repeated until all on-chip RAMs have been tested.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. D

7. Document ID: US 5689466 A

L9: Entry 7 of 12 File: USPT Nov 18, 1997

DOCUMENT-IDENTIFIER: US 5689466 A

**** See image for Certificate of Correction ****

TITLE: Built in self test (BIST) for multiple RAMs

Brief Summary Text (6):

Conventional BIST designs are typically capable of testing only one embedded RAM and utilize relatively complex techniques for generating data and predicting failure, usually involving collection of a signature for analysis. Furthermore, most BIST designs do not provide for detection of multibit faults.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

8. Document ID: US 5600658 A

L9: Entry 8 of 12 File: USPT Feb 4, 1997

DOCUMENT-IDENTIFIER: US 5600658 A

**** See image for Certificate of Correction ****

TITLE: Built-in self tests for large multiplier, adder, or subtractor

Brief Summary Text (8):

Many Built In Self Test (BIST) arrangements deal with embedded memory structures like Random Access Memories (RAMs). These arrangements usually tend to be implementation dependent and have rather complicated arrangements for generating data and predicting failures. In many cases, a signature is collected for analysis after a series of stimuli has been applied to the block being tested. Many BIST arrangements do not have the flexibility to be implemented with either software alone or hardware alone or a mixture of both. FIG. 2 depicts a typical self-test circuit. The logic block under test 201 has N independent logic inputs. An N-bit counter sequentially steps through all 2.sup.N unique input permutations. However, if it is desired for the self-test time to be less than about one second, N is typically limited to about twenty. The logic block under test has M output bits. An M-bit flip-flop 203 latches the output of after the first set of stimuli have been applied. Each subsequent M-bit output of the logic block is exclusive ORed with the contents of the flip-flop 203 such that at the end of the self-test, an M-bit signature is available as the output of the flip-flop 203. An exclusive OR 204 or exclusive NOR function is typically used because the its output value is always dependent upon all of the inputs. Therefore, if any single output of the logic block under test is incorrect, the final signature will be incorrect. (In contrast, a two-input AND function, for example, does not produce the same input-output dependence. For example, if one input of the AND function is zero, then the value of the other input does not influence the output at all.)

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

9. Document ID: US 5469445 A

L9: Entry 9 of 12 File: USPT Nov 21, 1995

DOCUMENT-IDENTIFIER: US 5469445 A

TITLE: Transparent testing of integrated circuits

Detailed Description Text (33):

In the case of the signature initialization algorithm the output response compaction will be performed by an Up/Down signature analyzer (or more generally by an Up/Down output response compactor), described later. The data read during the signature initialization algorithm (AL3*) are injected to the Up/Down output response compactor. Similarly to the signature prediction algorithm, some data of the algorithm AL3* (or alternatively some data of the algorithm AL3) are inverted

before to be injected to the compactor. The inverted data are the same as in the case of the signature prediction algorithm. During this phase the compactor is on the Down mode (resp. Up mode). Then, the data read during the basic transparent test algorithm (algorithm AL3) are injected to the compactor. During this phase the compactor is on the Up mode (resp. Down mode). According to the basic property of the Up/Down data compactors (see later), the final state of the output data compactor is equal to its initial state, and thus it is predictable.

Detailed Description Text (114):
In the case of the signature initialization algorithm the output response compaction will be performed by an Up/Down signature analyzer (or more generally by an Up/Down output response compactor), described later. The data read during the signature initialization algorithm are injected to the Up/Down output response compactor. Similarly to the signature prediction algorithm, some data of the signature initialization algorithm are inverted before to be injected to the compactor. The inverted data are the same as in the signature prediction algorithm. During this phase the compactor is on the Down mode (resp. Up mode). Then, the data read during the basic transparent test algorithm (table II) are injected to the compactor. During this phase the compactor is on the Up mode (resp. Down mode). According to the basic property of the Up/Down data compactors (see later), the final state of the output data compactor is equal to its initial state and thus it is predictable.

Detailed Description Text (145):
In the case of this scheme we will use an Up/Down output data compactor in order to obtain a predictable signature. During the Down (resp. the Up) mode, we compact the data read in the algorithm of table IV, and during the Up (resp. the Down) mode, we compact the data read in the algorithm of table II (some of these data have to be inverted as explained above). Since the data sequences injected to the data compactor during these modes, are the same but have reverse ordering, the final signature is equal to the initial state of the data compactor, and thus, it is predictable. This behaviour is due to the fact that we define an Up/Down data compactor to have the following property: if the state transition function of the Up mode is (data input=D.sub.q, present state=S.sub.q).fwdarw.next state=S.sub.q+1, then, in the Down mode, we will have (data input=D.sub.q, present state=S.sub.q+1).fwdarw.next state=S.sub.q. For instance, if we desire to use an Up/Down signature analyzer which, in the Up mode, behaves as an MISR, then, the Up/Down signature analyzer will be implemented by using an Up/Down LFSR as the ones described previously. In the Up mode, the signature analyzer works as a conventional MISR.

☐ 10. Document ID: JP 01010184 A

L9: Entry 10 of 12 File: JPAB Jan 13, 1989

DOCUMENT-IDENTIFIER: JP 01010184 A
TITLE: MULTICHIP PACKAGING STRUCTURE AND METHOD FOR TESTING IT

Abstract Text (2):
CONSTITUTION: A chip (UUT) to be tested is discriminated from a module. The interference between all other chips from which the UUT is separated and tests is electrically inhibited. The count of all patterns applied upon the UUT is fetched from a memory. A set of pseudo-random or weighted pseudo- random patterns is

propagated through the logic circuit of the UUT and becomes a predicted binary value which is found from the output of the UUT. The binary value is outputted from the UUT and accumulated in a signature analyzer and the accumulated result is sent to a comparator. A signature simulated for the UUT is inputted to the comparator from the memory and compared with an actual signature. Therefore, all chips of the module are tested and, when the diagnosis is completed, the process is stopped.

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

11. Document ID: NB900818

L9: Entry 11 of 12 File: TDBD Aug 1, 1990

TDB-ACC-NO: NB900818

DISCLOSURE TITLE: Pseudo-Random Pattern Self-Test of Arrays.

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, August 1990, US

VOLUME NUMBER: 33
ISSUE NUMBER: 3B
PAGE NUMBER: 18 - 19

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

12. Document ID: US 20030164835 A1

L9: Entry 12 of 12 File: DWPI Sep 4, 2003

DERWENT-ACC-NO: 2003-851951
DERWENT-WEEK: 200379

TITLE: Graphic system for signature analysis, has media processor to output requested and unrequested data, and hardware accelerator that has signature analysis register to capture requested and predictable data

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents

L8	12

Display Format: - Change Format

Previous Page Next Page Go to Doc#